ABSTRACT

A memory system includes a plurality of nonvolatile memory chips (CHP1 and CHP2) each having a plurality of memory banks (BNK1 and BNK2) which can perform a memory operation independent of each other and a memory controller (5) which can control to access each of said nonvolatile memory chips. The memory controller can selectively instruct either a simultaneous writing operation or an interleave writing operation on a plurality of memory banks of the nonvolatile memory chips. Therefore, in the simultaneous writing operation, the writing operation which is much longer than the write setup time can be performed perfectly in parallel. In the interleave writing operation, the writing operation following the write setup can be performed so as to partially overlap the writing operation on another memory bank. As a result, the number of nonvolatile memory chips constructing the memory system of the high-speed writing operation can be made relatively small.